IN THE CLAIMS:

Presented below are the claims in a clean, unmarked format. Please cancel Claims 1-29 without prejudice. Please add new Claims 30-49.

30. (New) A method comprising:

comparing a first voltage with a second voltage to determine whether said first voltage is greater than or less than said second voltage;

responding to said comparison by either:

increasing a charge pumping rate if said first voltage is less than said second voltage;

decreasing said charge pumping rate if said first voltage is greater than said second voltage; or

disabling charge pumping if said first voltage is much greater than said second voltage; and

generating a pumped voltage at a pump output in response to changes to said comparison response, wherein current is prevented from being supplied to an output node from said pump output if said pumped voltage is less than an output node voltage.

31. (New) The method of claim 30 further comprising pumping charge from a supply voltage to generate said pumped voltage, said pumped voltage having a higher voltage level than said supply voltage.

32. (New) The method of claim 30 further comprising dividing down said output node voltage to obtain said first voltage.

33. (New) The method of claim 32 wherein said increasing said charge pumping rate comprises increasing a frequency for a clock signal to a pump cell to achieve an increased pumped voltage.

34. (New) The method of claim 32 wherein said decreasing said charge pumping rate comprises decreasing a frequency for a clock signal to a pump cell to achieve a decreased pumped voltage.

35. (New) The method of claim 30 wherein said disabling charge pumping further comprises disabling said pump output.

36. (New) The method of claim 30 wherein said disabling charge pumping further comprises frequency blocking of clocking to a pump cell.

37. (New) An apparatus comprising:

a comparator to receive and compare a first voltage and a second voltage, said comparator to provide a first control signal;

a clock system coupled to said comparator, said clock system to generate clock signals in response to said first control signals;

a pump cell coupled to said clock system, said pump cell to generate a pumped voltage, wherein operation of said pump cell is controlled with said clock signals; and

a diode device coupled to a pump cell output, said diode device to monitor a pump output voltage and to control supplying of current from said pump cell to an output terminal, wherein charge from said output of said pump cell is not supplied to a pump output node if said pump output voltage is greater than at said pump cell output.

38. (New) The apparatus of claim 37 further comprising a feedback mechanism to couple said pump output voltage to said comparator.

39. (New) The apparatus of claim 38 further comprising a voltage divider coupled to said pump output node and said feedback mechanism, said voltage divider to divide said pump output voltage to a feedback voltage.

40. (New) The apparatus of claim 37 wherein said comparator is to further provide a second control signal and wherein said clock system is to further generate said clock signals in response to said second control signal.

41. (New) The apparatus of claim 40 wherein said first and second control signals are generated by said comparator in response to a comparison of said first voltage and said second voltage.

42. (New) The apparatus of claim 41 wherein said first voltage is a reference voltage and said second voltage is a feedback voltage derived from said pump output voltage.

43. (New) The apparatus of claim 41 wherein said clock system further comprises:

an oscillator coupled to said first control signal, said oscillator to generate an oscillating signal in response to said first control signal; and

a phase clock generator coupled to said oscillator and said second control signal, said phase clock generator to receive said oscillating signal and to generate a set of four phase clock signals based on a frequency of said oscillating signal.

44. (New) The apparatus of claim 43 wherein said first control signal is an analog signal, said first control signal to bias said oscillator to either increase or decrease said frequency of said oscillating signal.

45. (New) The apparatus of claim 44 wherein said second control signal is a digital signal, said second control signal to frequency block said phase clock generator by either enabling or disabling output of said four phased clock signals from said phase clock generator to said pump cell.

46. (New) An integrated circuit device comprising:

a memory array to store data;

decoding logic coupled to said memory array, said decoding logic to decode an address to access a location within said memory array; and

a charge pump coupled to said decoding logic, said charge pump to provide a high voltage supply for memory accesses, said charge pump comprising:

a comparator to receive and compare a first voltage and a second voltage, said comparator to provide a first control signal;

a clock system coupled to said comparator, said clock system to generate clock signals in response to said first control signals;

a plurality of pump cells coupled to said clock system, said plurality of pump cells to generate a pumped voltage, wherein operation of said plurality of pump cells is controlled with said clock signals; and

a diode device coupled to a pump output, said diode device to monitor a pump output voltage and to control supplying of current from said plurality of pump cells to an output node, wherein charge from said pump output is not supplied to said output node if said output voltage is greater than at said pump output.

47. (New) The integrated circuit device of claim 46 wherein said charge pump further comprises:

a feedback mechanism to couple said pump output voltage to said comparator; and

a voltage divider coupled to said pump output node and said feedback mechanism, said voltage divider to divide said pump output voltage to a feedback voltage.

48. (New) The integrated circuit device of claim 47 wherein:

said comparator is to further provide a second control signal;

said clock system is to further generate said clock signals in response to said second control signal; and

said first and second control signals are generated by said comparator in response to a comparison of said first voltage and said second voltage.

49. (New) The integrated circuit device of claim 48 wherein said clock system further comprises:

an oscillator coupled to said first control signal, said oscillator to generate an oscillating signal in response to said first control signal, wherein said first control signal is an analog signal to bias said oscillator to either increase or decrease said frequency of said oscillating signal; and

a phase clock generator coupled to said oscillator and said second control signal, said phase clock generator to receive said oscillating signal and to generate a set of four phase clock signals based on a frequency of said oscillating signal, wherein said second control signal is a digital signal to frequency block said four phased clock signals.